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A Leading Manufacturer of High Reliability Printed Circuit Boards

Common IPC-6012D/DS Requirement Differences Per Product Class

Characteristic	Class 2	Class 3	Class 3A*	IPC 6012D/DS Requirement UOS**
Annular Ring External PTH	90° Breakout Accepted Line width to meet Req.	50 µm [0.00197 in.] min. 20% isolated area reductions due to defects permitted	50 µm [0.00197 in.] min. 20% isolated area reductions due to defects permitted. Tear Drops AABUS	Table 3-9 / 3.4.2
Annular Ring Internal PTH	90° Breakout Accepted Line width to meet Req.	25 µm [0.00098 in.] min.	25 µm [0.00098 in.] min.	Table 3-9 / 3.6.2.1
Annular Ring, Unsupported Hole	90° Breakout Accepted Line width to meet Req.	150 µm [0.00591 in.] min.	150 µm [0.00591 in.] min.	Table 3-9 / 3.2.4
Burrs and Nodules	Accepted if minimum hole diameter and copper thickness is met			Table 3-10
Bow & Twist	Max. of 0.75% for Surface Mount Boards / 1.5% for all others			3.4.3
Cracks, Laminate	Cracks within and outside not > 80 µm [0.00315 in]			3.6.2.4
Cracks, Barrel / Corner	None Allowed			Table 3-10
Cracks, External Foil	Allowed if not extended into plating			Table 3-10
Cracks, Internal Foil	None Allowed			Table 3-10
Dielectric Thickness/Spacing	90 µm [0.00354 in.] min. unless specified			3.6.2.17
Lifted land (Visual)	None allowed on the delivered (non-stressed) printed board			3.6.2.10
De-wetting Solder Connection areas	5% Max	5% Max	None allowed*	3.5.4.5
	Conductors and planes are permitted			
Plating Thickness, Copper, Through, Blind, Buried Vias, >2 Layers, Average	20 µm [0.00079 in.] min.	25 µm [0.00098 in.] min.	25 µm [0.00098 in.] min.	3.6.2.11 Table 3-4
Plating Thickness, Copper, Through, Blind, Buried Vias, >2 Layers, Thin Areas	18 µm [0.00071 in.] min.	20 µm [0.00079 in.] min.	25 µm [0.00098 in.] min.*	3.6.2.11 Table 3-4
Plating Thickness, Copper, Through, Blind, Buried Vias, >2 Layers, Wrap	5 µm [0.00019 in.]	12 µm [0.00047 in.]	12 µm [0.00047 in.]	3.6.2.11 Table 3-4
Plating Thickness, Copper, Blind and Buried Microvias, Average	12 µm [0.00047 in.] min.	12 µm [0.00047 in.] min.	20 µm [0.00079 in.] min.*	3.6.2.11 Table 3-5
Plating Thickness, Copper, Blind and Buried Microvias, Thin Areas	10 µm [0.00039 in.] min.	10 µm [0.00039 in.] min.	18 µm [0.00071 in.] min.*	3.6.2.11 Table 3-5
Plating Thickness, Copper, Blind and Buried Microvias, Wrap	5 µm [0.00019 in.]	6 µm [0.00024 in.]	6 µm [0.00024 in.]	3.6.2.11 Table 3-5
Plating Thickness, Copper, Buried Via Cores (2 Layers), Average	15 µm [0.00059 in.] min.	15 µm [0.00059 in.] min.	20 µm [0.00079 in.] min.*	3.6.2.11 Table 3-6
Plating Thickness, Copper, Buried Via Cores (2 Layers), Thin Areas	13 µm [0.00051 in.] min.	13 µm [0.00051 in.] min.	18 µm [0.00071 in.] min.*	3.6.2.11 Table 3-6
Plating Thickness, Copper, Buried Via Cores (2 Layers), Wrap	5 µm [0.00019 in.]	7 µm [0.00027 in.]	7 µm [0.00027 in.]	3.6.2.11 Table 3-6
Nicks and Pinholes, Planes	Max. size is 1.0 mm [0.0394 in] with not more than 4 per side, per 625 sqcm [96.88 sqin]			3.5.4.1
Negative Etchback	25 µm [0.00098 in.]	13 µm [0.00051 in.]	None allowed*	3.6.2.8
Positive Etchback	Between 5 µm [0.000197 in.] and 80 µm [0.00315 in.] with preferred depth 13 µm [0.000512 in.]		Between 5 µm [0.000197 in.] and 40 µm [0.001574 in.] with preferred depth 13 µm [0.000512 in.]*	3.6.2.6
	The combination of dielectric removal from etchback plus wicking allowance **shall not** exceed the sum of the maximum allowable etchback or smear removal and the maximum allowable wicking limits in *Table 3-10 and as depicted in Figure 3-15.			
Surface Mount Lands	Defects along edge of land not > 20%; internal defects not > 10%			3.5.4.2.1
	Defects internal to the land remain outside central 80% of the diameter.			
Plating Separation	None Allowed			Table 3-10
Voids, Laminate	Voids within and outside thermal zone not > 80 µm [0.00315 in.]			3.6.2.3
Voids, Copper in Holes (Visual)	One per hole in not more then 5% of the holes	None allowed	None allowed at 3 diopters (approx. 1.75X)*	3.3.3 Table 3-7
Voids, Final Finish Plating (Visual)	Three per hole in not more the 5% of the holes	One per hole in not more then 5% of the holes	None allowed at 3 diopters (approx. 1.75X)*	
Nail Heading	Acceptable - indicator of process variation - alert management			3.6.2.19
Inner layer Inclusions/Separations	None Allowed			Table 3-10
Cap Plating of Filled Holes (Visual)	When cap plating of the filled holes is specified on the procurement documentation, plating voids exposing resin are not allowed, unless covered by solder mask. Must maintain structural integrity.			3.5.4.8
Cap Plating of Filled Holes Min.	5 µm [0.00019 in.]	12 µm [0.00047 in.]	12 µm [0.00047 in.]	3.6.2.11.2 Table 3-11
Cap Plating of Filled Holes Depression – max.	127 µm [0.005 in.]	76 µm [0.0030 in.]	76 µm [0.0030 in.] general areas	3.6.2.11.2 Table 3-11
			50 µm [0.0020 in.] in BGA areas	
Cap Plating of Filled Holes Protrusion – max.	50 µm [0.0020 in.]	50 µm [0.0020 in.]	50 µm [0.0020 in.]	3.6.2.11.2 Table 3-11
Electrodeposited Copper Tensile Strength	> 248 Mpa [36,000 PSI]	> 248 Mpa [36,000 PSI]	> 275.8 Mpa [40,000 PSI]	3.2.6.2 per IPC-TM-650 2.4.18.1
Electrodeposited Copper Elongation	> 12%	> 12%	> 18%	3.2.6.2 per IPC-TM-650 2.4.18.1

***Requirements for Class 3A product are referenced in IPC-6012DS.**

****UOS = Unless Otherwise Stated**

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